REMARKS

Applicant respectfully traverses and requests reconsideration.

Applicant wishes to thank the Examiner for the notice that claims 25-31 are allowed.

Claims 15-18 have been objected to due to informalities. The claims have been amended to correct the informalities.

Claim 17 stands rejected under 35 U.S.C. §112, 2nd paragraph as allegedly being indefinite. Applicant has amended claim 17 to correct typographical error.

Claims 1-7, 9-11 and 23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,341,347 (Joy) in view of Krishna. Joy is directed to thread switch logic in a multiple thread processor. As shown for example, in FIG. 3, two threads share a shared pipeline 314. Joy is silent as to the depth of the shared pipeline 314 and shows that the number of threads or programs are equal to two in FIG. 3.

Claim 1 requires, among other things, an execution pipeline having a depth less than or equal to a plurality of programs and having an average pipeline latency of one instruction per cycle. The claim also requires an interleaver for interleaving instructions from the plurality of programs and providing the instructions to the pipeline such that the number of programs that are interleaved is greater than or equal to the depth of the pipeline. The office action alleges that Joy teaches this claimed subject matter but does not teach that the pipeline has an average pipeline latency of one instruction per cycle. Krishna is allegedly cited as teaching this subject matter. Applicant respectfully submits that Joy does not teach what is alleged.

In particular, the office action states that Joy teaches a multiple thread execution pipeline that includes pipeline stages. The office action appears to mischaracterize the Joy reference by inadvertently confusing the description of a multi-processor embodiment with a single processor

embodiment. For example, the office action states that each pipeline stage can be immediately switched from a first thread to a second thread when the first thread stalls so a second thread is executing on an otherwise unused or idle pipeline stage. (See page 5 of office action citing to column 7, column 8, column 10, column 37). However, the cited portion of column 8 refers to "a single processor" and describe that the single processor does not switch threads to execute an otherwise unused or idle pipeline stage as alleged. Instead, it states that "when the active thread is stalled, the pipeline immediately switches to a non-stalled thread, if any and begins executing the non-stalled thread." (Column 8, lines 20-26). In other words, the thread is switched, not the pipeline. The cited portion of column 7 refers to a different and multiple processor embodiment wherein there are two processors, and thread switches can occur on otherwise "unused or idle pipeline" (column 7, lines 40-45). The office action however refers to unused or idle "pipeline stage" and confuses a pipeline stage with a plurality of pipelines on multiple processors. The Joy reference does not teach the claimed subject matter and in fact, is silent as to the pipeline depth. In addition, there is no mention of the number of programs that are interleaved to be greater than or equal to the depth of the pipeline as there is no discussion of the depth of the pipeline for a given shared pipeline. If the rejection is maintained, Applicant respectfully requests a showing as to the teaching of, inter alia, the actual depth of the pipeline versus the number of threads.

Since the office action inadvertently mischaracterizes Joy and since Joy does not teach what is alleged, Applicant respectfully submits that the claims are in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter.

The above relevant comments are also respectfully reasserted with respect to independent claim 23.

Claim 8 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Joy and Krishna in view of Nguyen. Applicant respectfully reasserts the relevant remarks made above and as such, this claim is also in condition for allowance.

Claims 12 and 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Joy and Krishna in view of Narayanaswami. Applicant respectfully reasserts the relevant remarks made above and as such, these claims are also in condition for allowance. The claims also add additional novel and non-obvious subject matter.

Claims 14-16 and 33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Joffe in view of Krishna. Applicant notes that it appears that among other differences Krishna does not teach scheduling amongst a plurality of programs and differing instructions from said programs. The claim is directed to interleaving instructions from multiple programs in a processor pipeline and wherein the pipeline has an average latency of one instruction per cycle and executing the instructions such that the first instruction from one of the programs is completed before beginning execution of the second instruction of a different program where no no-op or idle is inserted into the pipeline for purposes of insuring that the first instruction is completed before the beginning execution of the second instruction from a different program. What Krishna appears to be teaching as admitted in the office action is simply normal execution of an instruction from a single program is carried out with no no-op being inserted. Applicant claims a different operation and hence respectfully submits that the claims are in condition for allowance. Applicant also respectfully reasserts the relevant remarks made above and as such, this claim is also in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter.

As to claim 33, Applicant respectfully notes that this claim also requires, among other things, checking to see if all of said plurality of programs are completed. The office action cites column 2, lines 35-39 as allegedly teaching this subject matter. However, the cited portion does not refer to whether a plurality of identified programs have been completed, but to the contrary, refers to the fact that a resource is not provided to a task until after every other task sharing the resource has finished accessing the resource. The task may still be uncompleted but the resource is allocated as disclosed. As such, Applicant respectfully submits that if the rejection is maintained, that a non-final action be provided with an appropriate cite by column and line number to where Joffe teaches the claimed subject matter. Applicant respectfully submits that the claim is in condition for allowance.

Claim 17 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Joffe and Krishna in view of Narayanaswami. Applicant respectfully reasserts the relevant remarks made above and as such, this claim is also in condition for allowance.

Claim 18 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Joffe and Krishna in view of Nguyen. Applicant respectfully reasserts the relevant remarks made above and as such, this claim is also in condition for allowance.

Accordingly, Applicant respectfully submits that the claims are now in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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